EE330 HW3 Solutions

Problem 1

1) b) $Y = \overline{(AB+C)\cdot D}$ Compound gate approach

Pull Down n/w $\overline{Y} = (A\cdot B+C)\cdot D$

Pull up n/w $\overline{\overline{Y}} = \overline{(A\cdot B+C)} + \overline{D}$

$= ((\overline{A\cdot B})\cdot \overline{C}) + \overline{D}$

$= ((\overline{A}+\overline{B})\cdot \overline{C}) + \overline{D}$

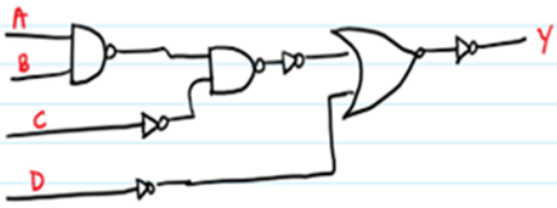
Total no of transistors = 8

Number of logic gates = 1 level of logic

Static CMOS Gate

$Y = \overline{(AB+C)\cdot D} = \overline{(AB+C)} + \overline{D}$

$= (\overline{AB}\cdot \overline{C}) + \overline{D}$

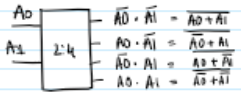


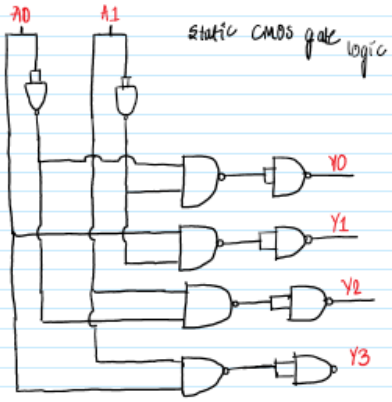
Total no of transistors = 20

Number of logic gates = 5 level of logic

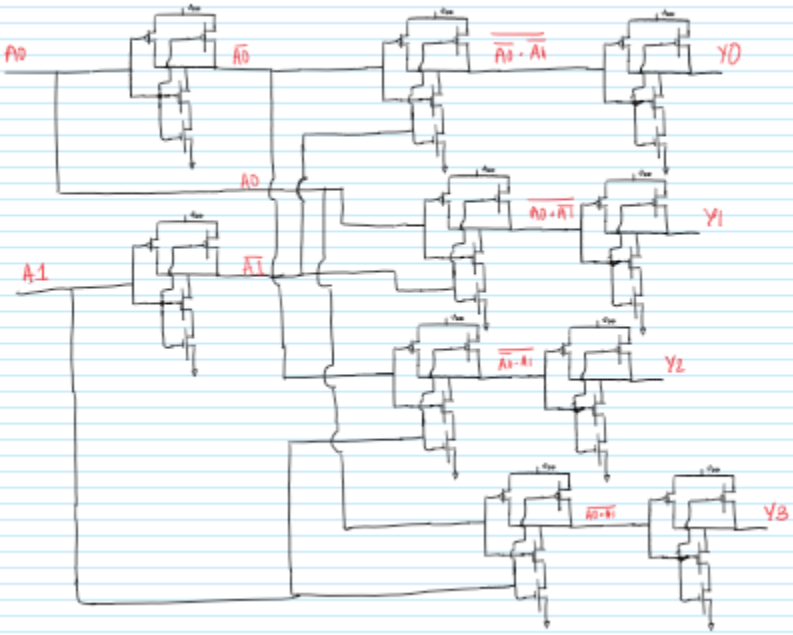
Problem 2

2)

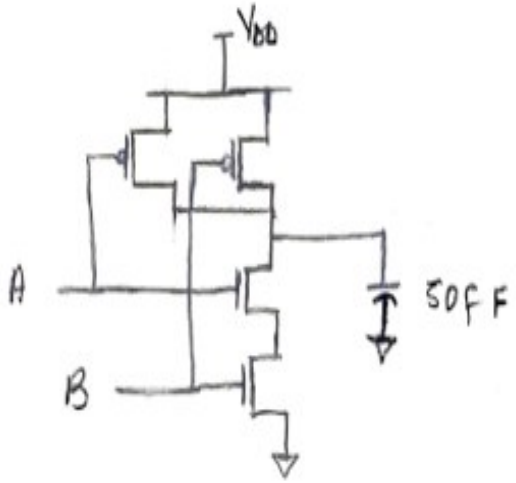


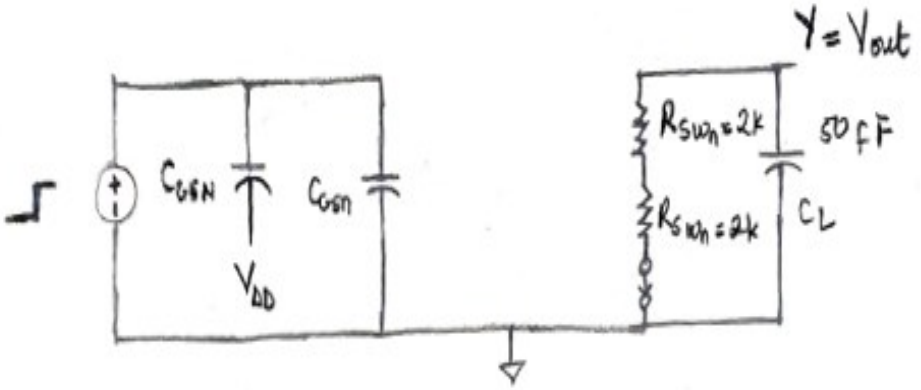


transistor level logic.



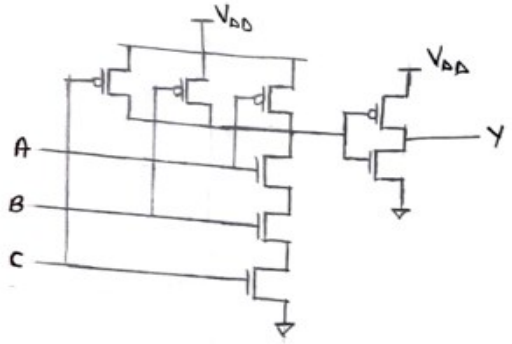
Problem 3

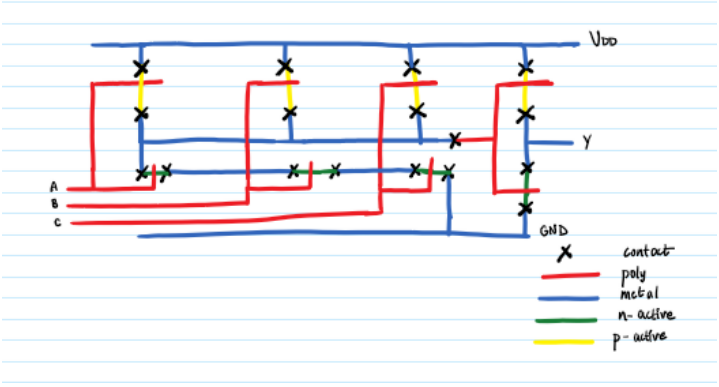




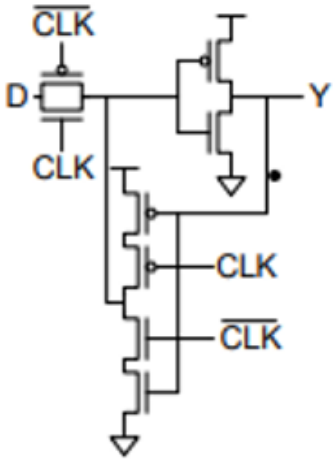
$$\Rightarrow t_{HL} = R_{Swn} C_L = (2k + 2k)\ 50 \times 10^{-15} = \underline{2 \times 10^{-10}\ \text{seconds}}$$

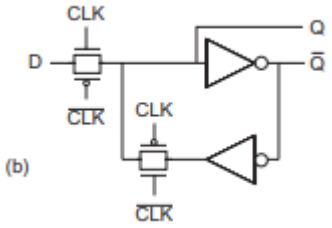
Problem 4





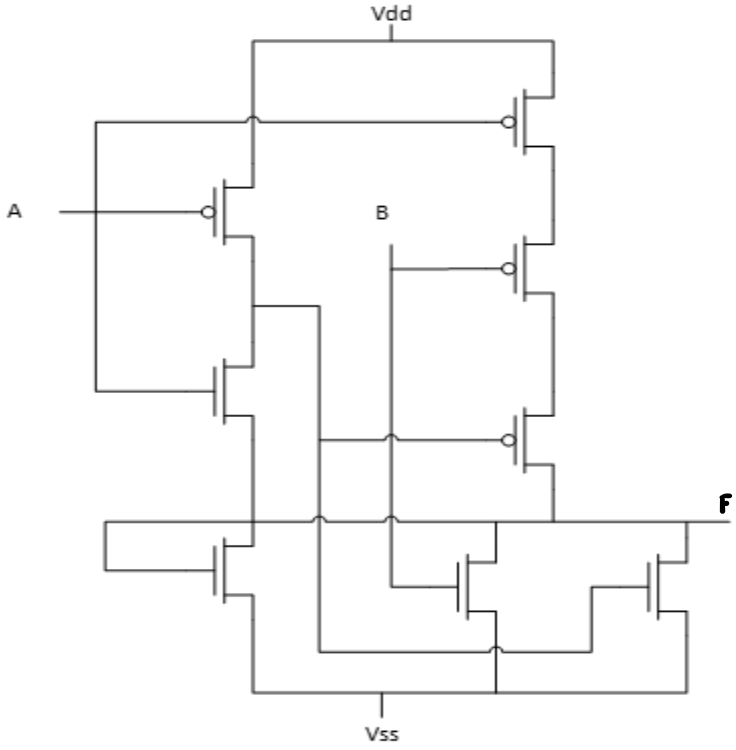
Problem 5





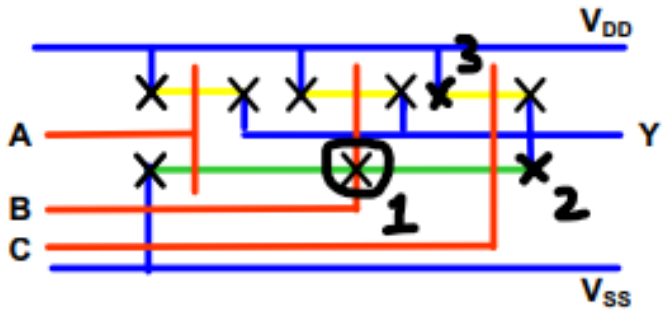
We can see that the figure of 1.31b) has 2 not gates and 2 T-gates.

Problem 6



Problem 7

For this stick diagram there are 3 errors:



1. No need of contact poly to n-active.
2. Contact needed for Metal 1 to n-active.
3. Contact needed for Metal 1 to p-active.

Problem 8

Assuming ON 0.18μm process, $C_{IN} = 1.5fF$, $R_{SWP} = 6k\Omega$, and $R_{SWN} = 2k\Omega$

Total C_{IN} of 6 driven inverters = C_{IN} * 6 inverters * 2 transistors/inverter = 18fF = C_L

If input steps from 2V to 0V, the transition at output will be from 0V to 2V, so we will be calculating t_{LH}

From lecture, $t_{LH} = C_L * R_{SWP} = 18fF * 6k\Omega = 108$ picoseconds

Problem 9

For this problem, there are three concepts to keep in mind

- Any interconnect will act as a resistor
- Conductivity is the inverse of resistivity
- Interconnect area = $5\mu m * 0.2\mu m = 1\mu m^2$

a) Resistivity of aluminum = $\frac{1}{38}\frac{ohm}{\mu m}$

Resistance = $\frac{\rho L}{A}$

Resistance of first segment = $\frac{1/_{38*(180+40)}}{1} = \frac{220}{38} = 5.7895\ ohms$

Resistance of second segment = $\frac{1/_{38*(80)}}{1} = \frac{80}{38} = 2.1053\ ohms$

The voltage across the resistor = $2V * \frac{50\ ohms}{(50+5.7895+2.1053)ohms} = 1.727V$

b) Resistivity of copper = $\frac{1}{58}\frac{ohm}{\mu m}$

Resistance = $\frac{\rho L}{A}$

Resistance of first segment = $\frac{1/_{58*(180+40)}}{1} = \frac{220}{58} = 3.7931\ ohms$

Resistance of second segment = $\frac{1/_{58*(80)}}{1} = \frac{80}{58} = 1.3793\ ohms$

The voltage across the resistor = $2V * \frac{50\ ohms}{(50+3.7931+1.3793)ohms} = 1.813V$

Problem 10

```
/*structural implementation of f=(!a*b*c)+(a*b*!c)
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`timescale 1ns/1ps                  //set timescale to something nice for simulation
module hw3q10(A, B, C, F);          //define module and IO
       input A, B, C;               //define A, B, and C as inputs
       output F;                    //define F as an output
       wire and1, and2;             //define intermediary wires to be used
       and(and1, ~A, B, C);         //and1 = A!*B*C
       and(and2, A, B, ~C);         //and2 = A*B*!C
       or(F, and1, and2);           //F = and1 + and2 = (A!*B*C) + (A+B+!C)
endmodule                           //end the module
/*behavioral implementation of f=(!a*b*c)+(a*b*!c)
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`timescale 1ns/1ps                          //set timescale to something nice for simulation
module hw3q10(A, B, C, f);                  //define module and IO


       input A, B, C;                       //define A, B, and C as inputs
       output F;                            //define F as an output
       reg out;                             //define an output register for used
       assign F = out;                      //assign output register to given output
       always @ (A or B or C) begin         //when inputs change, execute the following
              out = (~A&B&C) + (A&B&~C);    //f = (!A*B*C)+(A*B*!C)
       end                                  //end of preceding always block
endmodule                                   //end the module
/*standard 3-input logic testbench
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Nickolas Moser
February 2, 2022*/

`timescale 1ns/1ps                          //set timescale to something nice to simulate

module standard_tb();                       //instantiate testbench module
```

```
        reg a_in, b_in, c_in;                       //define input registers
        wire out;                                   //define output wire
        hw3q10 DUT(.A(a_in), .B(b_in), .C(c_in), .F(out));   //instantiate Device Under Test
                initial a_in = 0;                   //set initial input values
                initial b_in = 0;
                initial c_in = 0;
                always  #1 a_in = ~a_in;            //for input n, toggle every 2^n time units
                always  #2 b_in = ~b_in;
                always  #4 c_in = ~c_in;
endmodule                                           //end testbench module
```